What is claimed is:

1. A method for forming a storage node contact of a semiconductor device, comprising the steps of:

depositing sequentially a conductive layer, a nitride layer and a polysilicon layer on a substrate having an insulating structure and a conductive structure;

etching selectively the polysilicon layer, the nitride layer and the conductive layer to form a plurality of conductive patterns with a stack structure of the conductive layer and a dual hard mask including the polysilicon layer and the nitride layer;

forming an insulation layer along a profile containing the conductive patterns; and

etching the insulation layer by using a line type photoresist pattern as an etch mask to form a contact hole exposing the conductive structure disposed between the neighboring conductive patterns.

2. The method as recited in claim 1, after the step of forming the contact hole, further including the steps of:

depositing an oxide layer along a profile containing the contact hole; and

forming a spacer at sidewalls of each conductive pattern by etching the oxide layer through a blanket etch-back process.

3. The method as recited in claim 1, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the conductive patterns are formed.

4. The method as recited in claim 1, wherein the nitride layer has a thickness ranging from about 900 Å to about 1500 Å.

5. The method as recited in claim 1, wherein the conductive pattern is one of a bit line, a gate electrode and a metal wire.

6. The method as recited in claim 1, wherein the conductive layer is made of a material selected from a group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

7. The method as recited in claim 1, wherein the plug is formed with one of polysilicon and titanium nitride.

8. The method as recited in claim 1, the insulation layer is made of a material selected from a group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass

(SOG).

9. The method as recited in claim 1, further comprising the steps of removing the photoresist pattern after the step of forming the contact hole.

10. The method as recited in claim 1, wherein at the step of forming the photoresist pattern, photolithography using a light source of ArF or KrF is used to form the photoresist pattern.

11. The method as recited in claim 1, further comprising the steps of:

depositing a plug material into the contact hole so that the plug material is contacted to the exposed conductive structure; and

removing the plug material, the insulation layer and the polysilicon layer in a manner of exposing the nitride layer to form a plurality of plugs planarized at the same surface level of the exposed nitride layer.

12. A method for fabricating a semiconductor device, comprising the steps of:

depositing sequentially a bit line conductive layer, a nitride layer and a polysilicon layer on a substrate in which a first plug is formed;

etching selectively the polysilicon layer, the nitride layer and the bit line conductive layer to form a plurality of bit lines with a stack structure including the conductive layer and a hard mask with a dual structure of the polysilicon layer and the nitride layer;

forming an insulation layer along a profile containing the bit lines; and

etching the insulation layer by using a line type photoresist pattern as an etch mask to form a contact hole exposing the first plug disposed between the bit lines.

13. The method as recited in claim 12, after the step of forming the contact hole, further including the steps of:

depositing an oxide layer along a profile containing the contact hole; and

forming a spacer at sidewalls of each bit line by etching the oxide layer through a blanket etch-back process.

14. The method as recited in claim 12, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the bit lines are formed.

15. The method as recited in claim 12, wherein the nitride layer has a thickness ranging from about 900 Å to

about 1500 Å.

16. The method as recited in claim 12, wherein the conductive layer is made of a material selected from a group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

17. The method as recited in claim 12, the insulation layer is made of a material selected from a group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass (SOG).

18. The method as recited in claim 12, further comprising the steps of:

depositing a plug material into the contact hole so that the plug material is contacted to the exposed first plug; and

removing the plug material, the insulation layer and the polysilicon layer in a manner of exposing the nitride layer to form a plurality of second plugs planarized at the same surface level of the exposed nitride layer.